CLAIMS

What is claimed is:

1. A device comprising:

a network processor including a flow control message First In First Out (FIFO) buffer and wherein said FIFO buffer includes a parity field and wherein when said network processor detects a parity error on a read from said FIFO buffer, said network processor corrupts at least one of horizontal parity, vertical parity and Diagonal Interleaved Parity (DIP-2) code.

2. The device of claim 1 further comprising a Control and Status Register (CSR) and wherein an error bit is set in said CSR when a read from said FIFO buffer results in a parity error.

3. The device of claim 1 wherein when said network processor detects a parity error on a read from said FIFO buffer, said network processor asserts an error signal, pushes corrupted data to a device in communication with said network processor and flushes said FIFO buffer.

4. The device of claim 1 wherein said network processor comprises an Egress network processor and wherein said FIFO buffer comprises a Flow Control Egress First In First Out (FCEFIFO) buffer.

5. The device processor of claim 1 wherein said network processor comprises an Ingress network processor and wherein said FIFO buffer comprises a Flow Control Ingress First In First Out (FCIFIFO) buffer.

6. The device of claim 1 wherein said flow control message comprises a Common Switch Interface (CSIX) flow control message.

7. The device of claim 1 wherein said flow control message comprises a Network Processor Streaming Interface (NPSI) Network Processing Engine (NPE) -Fabric flow control message

8. A method of handling parity errors in flow control channels comprising:

receiving a flow control message at an Egress network processor;

storing said flow control message and a parity bit in an FCEFIFO buffer;

reading said flow control message from said FCEFIFO;

determining whether there was a parity error during said read from said FCEFIFO, and when a parity error resulted from said read then setting an error bit in an Egress CSR and corrupting parity associated with said message; and

sending said flow control message out of said Egress network processor.

9. The method of claim 8 wherein said corrupting parity associated with said error message comprises corrupting at least one of horizontal parity, vertical parity and DIP-2 code.

10. The method of claim 8 wherein said receiving a flow control message comprises receiving a CSIX flow control message.

11. The method of claim 8 wherein said receiving a flow control message comprises receiving a NPSI NPE-fabric flow control message.

12. The method of claim 10 wherein said sending said flow control message out of said Egress network processor comprises sending said flow control message to an Ingress network processor.

13. The method of claim 11 wherein said sending said flow control message out of said Egress network processor comprises sending said flow control message to a switch fabric.

14. A method of handling parity errors in flow control channels comprising:

receiving a flow control message at an Ingress network processor;

storing said flow control message and a parity bit in an FCIFIFO buffer;

reading said flow control message from said FCIFIFO;

determining whether there was a parity error during said read from said FCIFIFO, and when a parity error resulted from said read then setting an error bit in an Ingress CSR, pushing corrupted data out of said Ingress NP and flushing said FCIFIFO; and

sending said flow control message out of said Ingress network processor when said read from said FCIFIFIO did not result in a parity error.

15. The method of claim 14 wherein said receiving a flow control message comprises receiving a CSIX flow control message.

16. The method of claim 14 wherein said receiving a flow control message comprises receiving a NPSI NPE-fabric flow control message.

17. The method of claim 14 wherein said sending said flow control message out of said Ingress network processor comprises sending said flow control message to a peripheral device.

18. An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

receiving a flow control message at an Egress network processor;

storing said flow control message and a parity bit in an FCEFIFO buffer;

reading said flow control message from said FCEFIFO;

determining whether there was a parity error during said read from said FCEFIFO, and when a parity error resulted from said read then setting an error bit in an Egress CSR and corrupting parity associated with said message; and

sending said flow control message out of said Egress network processor.

19. The article of claim 18 wherein said corrupting parity associated with said error message comprises corrupting at least one of horizontal parity, vertical parity and DIP-2 code.

20. The article of claim 18 wherein said receiving a flow control message comprises receiving a CSIX flow control message.

21. The article of claim 18 wherein said receiving a flow control message comprises receiving a NPSI NPE-fabric flow control message.

22. The article of claim 20 wherein said sending said flow control message out of said Egress network processor comprises sending said flow control message to an Ingress network processor.

23. The article of claim 21 wherein said sending said flow control message out of said Egress network processor comprises sending said flow control message to a switch fabric.

24. An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

receiving a flow control message at an Ingress network processor;

storing said flow control message and a parity bit in an FCIFIFO buffer;

reading said flow control message from said FCIFIFO;

determining whether there was a parity error during said read from said FCIFIFO, and when a parity error resulted from said read then setting an error bit in an Ingress CSR, pushing corrupted data out of said Ingress NP and flushing said FCIFIFO; and

sending said flow control message out of said Ingress network processor when said read from said FCIFIFIO did not result in a parity error.

25. The article of claim 24 wherein said receiving a flow control message comprises receiving a CSIX flow control message.

26. The article of claim 24 wherein said receiving a flow control message comprises receiving a NPSI NPE-fabric flow control message.

27. The article of claim 24 wherein said sending said flow control message out of said Ingress network processor comprises sending said flow control message to a peripheral device.

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